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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,552	09/22/2003	Wolfgang Dettman	04020-P0005A	9996

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EXAMINER	
ROSASCO, STEPHEN D	
ART UNIT	**PAPER NUMBER**
1756	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,552	DETTMAN ET AL.	
	Examiner	Art Unit	
	Stephen Rosasco	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/16/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ho (6,569,584) or Choi (6,821,688) in view of Tomita (6,521,969).

The claimed invention is directed to a mask for the production of semiconductor devices, comprising at least one product field area (6a) and a compensation structure (5) positioned outside the product field area (6a) characterized in that the compensation structure (5) comprises at least one electroconductive region (8b) which is electrically connected with the product field area (6a).

And wherein--viewed from the product field area (6a)--the electroconductive region (8b) extends path-shaped outwardly.

And wherein the path (8b) of the electroconductive region has a breadth (d) of between 1 nm and 30 mm or 200 nm and 5 mm, respectively, in particular between 1-50 mum.

And comprising a plurality of, in particular more than 10, 100, 1,000 or 10,000, electroconductive regions (8a, 8b) that are electrically connected with the product field area (6a).

And wherein the plurality of electrical regions (8a, 8b) form a grid structure and are made of chrome.

The applicant states that an advantage of this design is that by the electrical connection of the product field area with an outward area of the mask, electrostatic charging is minimized, and an increased steadiness of the process conditions during the performance of the etching processes or plasma etching processes, respectively, is achieved (this making it possible to increase the manufacturing accuracy).

Ho et al. teach a reticle and a method for optically transferring a lithographic mask pattern from a reticle onto a semiconductor substrate in accordance with an integrated circuit fabrication process defining a critical dimension, the method comprising: forming the reticle such that the lithographic mask pattern includes a first mask line and a dummy mask pattern, the dummy mask pattern including a first plurality of dummy mask portions arranged parallel to the mask line, wherein each dummy mask portion of the first plurality of dummy mask portions is separated from the mask line by an offset distance that corresponds to the critical dimension of the integrated circuit fabrication process and wherein each dummy mask portion of the first plurality of dummy mask portions is electrically isolated from all other dummy mask portions of the first plurality of dummy mask portions and all mask lines of the lithographic mask pattern; and transferring an image of the lithographic mask pattern onto the semiconductor substrate during the

integrated circuit fabrication process to form a line on the semiconductor substrate that corresponds with the mask line.

Choi teaches a photomask comprising a mask substrate formed of a transparent nonconductor; a plurality of opaque conductive patterns formed on the mask substrate and separated from one another; and one or more conductive lines for connecting one of the conductive patterns with at least one adjacent conductive pattern, wherein the conductive lines have a thickness and a width that allow incident light to be transmitted, the width being less than half the wavelength of an ion source used in the FIB system, a thickness of the conductive lines being less than a skin depth.

And wherein the conductive patterns comprise chromium (Cr).

The teachings of the cited are differ from those of the applicant in that the applicant teaches that the applicant teaches specific numbers of conductive lines and shapes of regions (claims 5-13).

Tomita teaches a semiconductor device comprising: a semiconductor substrate; electrical active device regions formed in the semiconductor substrate; and an isolating region made of a trench-type isolating oxide film, of which surface is abraded by a CMP method, wherein: a plurality of types of dummy patterns having various areas, including first dummy patterns having relatively small areas of the same size and second dummy patterns having relatively large areas of a size larger than the size of the relatively small areas, being active regions of a dummy

surrounded by the trench-type isolating oxide film patterns, are located in the isolating region so that the trench-type isolating oxide film pattern does not exceed a predetermined width; the dummy patterns are regularly arranged by setting an area in response to a positional relationship between the dummy patterns and patterns of the electrical active device regions; the first dummy patterns having relatively small areas are arranged around the entire periphery of at least one of the electrical active device patterns; and the second dummy patterns having the relatively large areas are arranged around the first dummy patterns having the relatively small areas.

Tomita also teaches that the dimensions of the small dummy patterns 11a are appropriately set within a range of 1 through 100 times of the minimum dimensions of the actual patterns 9. The dimensions of the large dummy patterns 11b are appropriately set within a range of 10 through 1,000 times of the minimum dimension of the actual patterns 9. The dummy patterns 11, i.e. the small dummy patterns 11a and the large dummy patterns 11b, may be shaped like not only a rectangular but also a strap, a hook, and lines and spaces as long as the dummy patterns are regularly arranged to facilitate a control of process.

It would have been obvious to one having ordinary skill in the art to take the teachings of Ho et al. or Choi and combine them with the teachings of Tomita in order to make the claimed invention because Tomita teaches a comparable number

of conductive lines and it would be well known that the shape of regions is a function of the specific pattern that is to be formed.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Rosasco
Primary Examiner
Art Unit 1756

S.Rosasco
08/02/05